In the Specification:

Please amend the specification as set forth below.

Please insert the following paragraph between the paragraph starting on pg. 11, line 7 and the paragraph starting on pg. 11, line 12:

Fig. 2d shows a gate electrode f, a landing plug g, a first interlayer insulating film h, and a second interlayer insulating film I.

The paragraph starting on page 12, line 12:

Thereafter, the lower insulating layer 41 is etched via a photolithography process using a landing plug contact mask (not shown) to form a landing plug contact hole 43 exposing an active region of the semiconductor substrate. A polysilicon layer (not shown) filling the landing plug contact hole 43 is formed on the entire surface of the resulting structure, and then planarized to form a landing plug ~~plug 45~~. The planarization process is performed using the hard mask layer on the gate electrode as etch barrier layer to form the landing ~~plug 45~~ plug connected to the active region between the gate electrodes where a storage electrode or a bit line is to be contacted.

The paragraph starting on page 13, line 21:

Next, a third interlayer insulating film (not shown) is deposited on the entire surface of the resulting structure. The third insulating film and the first interlayer insulating film are etched using a storage electrode contact mask (not shown) to form a storage electrode contact hole 57 exposing the landing plug ~~plug 45~~.

The paragraph starting on page 15, line 6:

Referring to Fig. 4d, an etching process is performed to remove the over-hang and the second nitride film 61 at the bottom of the storage electrode contact hole 57 to expose the landing plug ~~plug 45~~.

In the Title

Please replace the title with "Method for Forming a Semiconductor Device with a Hard Mask Layer Formed Over a Bit Line to Protect the Bit Line During Subsequent Etching Steps."